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sercos EasySlave-IO

Design Guide

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Abstract:
This document describes requirements for a sercos EasySlave PCB design.

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19.07.2012	0.1	Document created	C. Hayer
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Contents

1 Definitions and abbreviations

Definition	Description
FPGA	Field-programmable gate array is a device where the logic network can be programmed into the device after its manufacture. An FPGA consists of an array of logic elements, either gates or lookup table RAMs, flip-flops and programmable interconnect wiring.
sercos III	third generation sercos is an industrial standard which specifies real-time Ethernet communication for automation.
EasySlave	A free IP core for low-cost FPGA chips, which allows SERCOS III to be integrated into basic I/O slave devices with minimal development and integration effort.
FSP IO	Function Specific Profile IO is a sercos III device profile for I/O applications.
S/IP	All IPS services, which are based on TCP and UDP.
TFTP	Trivial File Transfer Protocol is a very simple file transfer protocol which is typically based on UDP.
SDDML	sercos Device Description Markup Language is a markup language, which contains sercos III-defined tags, in order to describe the functionality that a sercos III device supports, in the form of an XML file.
IDN	Identification number of a SERCOS parameter.
UCC channel	Unified Communication Channel, Standard Ethernet Frames like UDP & TCP will be transmitted and services like Ping will be transmitted also.
RT channel	Real-time channel is a certain time span of the communication cycle in which real-time telegrams are sent.
Ethernet	A widely used type of local area network and compatible to ISO/IEC 8802-3 standard.
Hot-plug	Possibility to insert a slave in the sercos III network, inclusive its initialization, while the sercos III network is running.

2 Introduction

2.1 sercos – the automation bus

Industrial Ethernet has become the de facto standard for manufacturing information networking, and the market is requesting Ethernet connectivity for servo drives. Ethernet offers high-speed data throughput at 10-100 times faster than fieldbus solutions. It uses standard off-the-shelf components and cabling and offers consistent IT implementation from office to the machine level. The problem is that Industrial Ethernet is characterized by high bandwidth and low hardware costs, but is not deterministic. Office communications and certain single-axis motion applications can tolerate delays and data re-transmissions, but that would be disastrous for coordinated multi-axis robots or high-speed machine tools.

The sercos automation bus, on the other hand, is optimized for high-speed deterministic motion control, which is required for the exact synchronization of multiple drives. Sercos also defines a protocol structure and includes an ample variety of profile definitions for control of motion and I/O devices.

Sercos III is the open, IEC-standardized third-generation of sercos that "right engineers" Industrial Ethernet for real-time control, combining the best of both Ethernet and previous Sercos designs to provide the highly deterministic bi-directional real time motion and I/O control required by modern production equipment. It overcomes the wasted bandwidth in other TCP/IP-based Ethernet bus solutions, because it is based directly on Ethernet frames, defining a new, registered EtherType for sercos. In addition to real-time communications between all drives and the motion control, sercos III provides rich I/O communication capabilities, while also enabling other protocols, such as EtherNet/IP, TCP/IP, UDP and others, to be transmitted over the same Ethernet network efficiently in parallel with sercos real-time communication. Sercos III is a truly a universal automation bus for machine production and system implementation.

Sercos III offers several fundamental performance and technology benefits for OEMS and end-users:

- Cycle times as low as 31.25 microseconds.
- High speed: it uses Fast Ethernet (100 Mb/s).
- Support for either line or ring topologies; in addition hierarchical, synchronized and real-time coupled network structures can be implemented.
- Support for up to 511 slave devices in one network, with multiple networks possible in a system.
- Bumpless cable break recovery in ring mode within 25 usec.
- Advanced cross communications—both slave-to-slave and controller-to-controller (sometimes called machine-to-machine).
- Capable of hot-plugging devices and network segments—adding machine or line components to a network with synchronization up and running, without having to reset the network or cycle power.
- Support for safety functions up to SIL3 according to IEC 61508 via CIP Safety for sercos.
- I/O profile that provides an XML-based device and profile description language for I/O device configuration.
- Energy profile that defines parameters and commands for the reduction of energy consumption in a uniform vendor-independent manner.
- Encoder profile that provides a standard method to integrate encoders into a sercos III network.
- Lower hardware costs.

There are several key advantages that manufacturers, systems engineers and machine builders can leverage when using sercos III—advantages that enable drive and control systems with vastly improved flexibility and performance.

2.2 sercos EasySlave

The sercos EasySlave is an FPGA-based single-chip controller, enabling inexpensive development of simple sercos III slave devices such as I/O. I/O applications are synchronized in the sercos cycle. An IP core is provided as a netlist for the Xilinx Spartan-6 FPGA family. The IP core contains all the functions of a sercos slave connection, including the associated software library for I/O devices (e.g., analog inputs, encoders). The user can add IP cores for I/O from Xilinx and his own application code and can integrate the controller into his own board. A reference design is available.

Technical support for the EasySlave is provided by Steinbeis-Transferzentrum Systemtechnik (TZS) in Esslingen, Germany. TZS offers an EasySlave evaluation kit to facilitate a quick and easy introduction to Sercos slave development. The evaluation kit includes a development board based on a Xilinx Spartan-6 XC6SLX16/25 FPGA and can be extended using plug-in modules. The evaluation kit includes all other required material and documents (Ethernet cable, power supply, and documentation). Steinbeis-TZS can provide assistance in the integration and commissioning of EasySlave.

Features and Specifications for EasySlave FPGA-based Single-Chip Controller

- FPGA-based single chip controller containing a reduced sercos slave IP core
- Target devices: analog/digital I/Os, simple sensors and actuators
- FPGA-internal RAM for sercos stack, application and data
- Real-time channel with max. 32 bytes output and max. 32 bytes input data (1 input and 1 output connection)
- Supported cycle times down to 31.25 µs
- Synchronization of application to sercos cycle
- Parameterization over service channel
- Hot-plug support
- Service channel with hardware support
- IP channel for ARP, Ping and firmware update over TFTP
- Design currently targeted to Xilinx Spartan-6 FPGA series
- FPGA reference design (Xilinx EDK V13.4) and Software-API (Xilinx MicroBlaze / gcc) available

Various EasySlave licensing models are available from sercos international, with sercos member companies offered special prices. In addition, a license-free IP core version (loaded with a bitstream IP core) with a limited functionality is available, under the product name EasySlave-IO.

3 Recommendations and Sources

3.1 Recommendations

Software Tool:
XILINX ISE 13.4 EDK

Device:
XILINX Spartan-6 XC6SLX16 or higher density

FPGA device type	EasySlave-IO [1)]
Slice Registers	4907 of 30064 (16%)
4 input LUTs	6042 of 15032 (34%)
Number of IOBs	111 of 186 (59%)
Block RAMs	40 of 52 (76%)
Speed Grade	-2

1) Results by using design ISE 13.4

3.2 Source files

Slave design:
S3_ESLV_IO_XC6SLX16-FT256_V1_0_0.ucf

4 Guidelines

4.1 Power supply

The EasySlave requires two supply voltages:

- 3,3V for Vcc and I/O supply > current rating 500mA
- 1,2V for FPGA core supply > current rating 100mA

Required PCB capacitor quantities per FPGA device [X1]

Package	Device (XC6S)	V_{CCINT} in µF			V_{CCAUX} in µF			V_{CCO} Bank 0 in µF			V_{CCO} Bank 1 in µF			V_{CCO} Bank 2 in µF			V_{CCO} Bank 3 in µF			Total
		100	4.7	0.47	100	4.7	0.47	100	4.7	0.47	100	4.7	0.47	100	4.7	0.47	100	4.7	0.47	
FT(G)256	LX16	0	5	1	1	1	2	1	1	1	1	1	2	1	1	1	1	1	2	24
FT(G)256	LX25	1	1	1	1	1	2	1	1	1	1	1	2	1	1	1	1	1	2	21

Ideal Value	Value Range(1)	Body Size(2)	Type	ESL Maximum	ESR Range(3)	Voltage Rating(4)	Suggested Part Number
100 µF	C > 100 µF	1210	2-Terminal Ceramic X7R or X5R	5 nH	10 mΩ < ESR < 60 mΩ	6.3V	GRM32ER60J107ME20L
4.7 µF	C > 4.7 µF	0805	2-Terminal Ceramic X7R or X5R	2 nH	10 mΩ < ESR < 60 mΩ	6.3V	
0.47 µF	C > 0.47 µF	0204 or 0402	2-Terminal Ceramic X7R or X5R	1.5 nH	10 mΩ < ESR < 60 mΩ	6.3V	

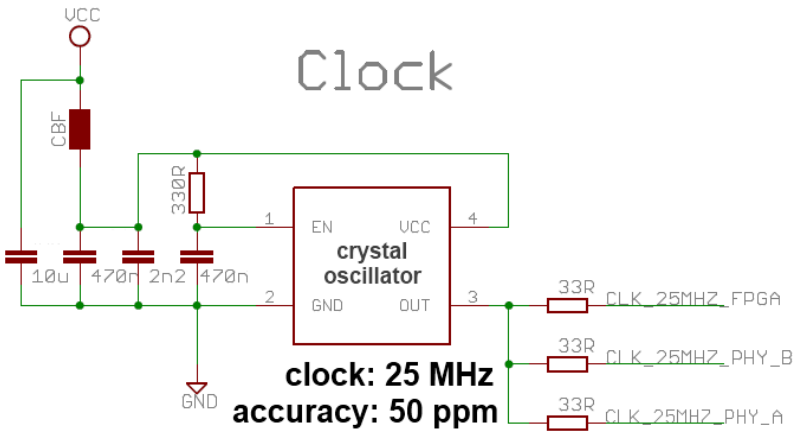
PCB Capacitor Substitution Rules:

1. Values can be larger than specified.
2. Body size can be smaller than specified.
3. ESR must be within the specified range.
4. Voltage rating can be higher than specified.

To perform the decoupling function, capacitors should be close to the device being decoupled.

4.2 Clock

The EasySlave requires a 25 MHz crystal oscillator with an accuracy of 50 ppm or better. The clock signal shall be decoupled by serial resistors.



4.3 FPGA design

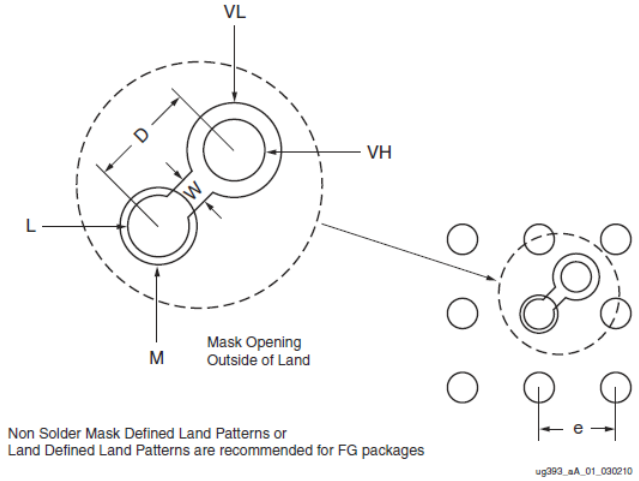
4.3.1 PCB Layout

The EasySlave is based on a FPGA with a BGA package. For fan-out the signals of the FPGA in minimum 6 PCB layers are required for the EasySlave-IO, 8 PCB layers are recommended.

Some PCB design parameters:

Minimum wire width: 0.13 mm
Minimum clearance: 0.13 mm
Minimum via drill: 0.2 mm
No micro via or blind vias required

Xilinx provides the diameter of a land pad on the component side. This information is required prior to the start of the board layout so the board pads can be designed to match the component-side land geometry. The typical values of these land pads are following described. [X3]



Design Rule	FT(G)256
Component land pad diameter (SMD)(1)	0.40
Solder land (L) diameter	0.40
Opening in solder mask (M) diameter	0.50
Solder (ball) land pitch (e)	1.00
Line width between via and land (w)	0.13
Distance between via and land (D)	0.70
Via land (VL) diameter	0.61
Through hole (VH) diameter	0.300

6 layer stackup

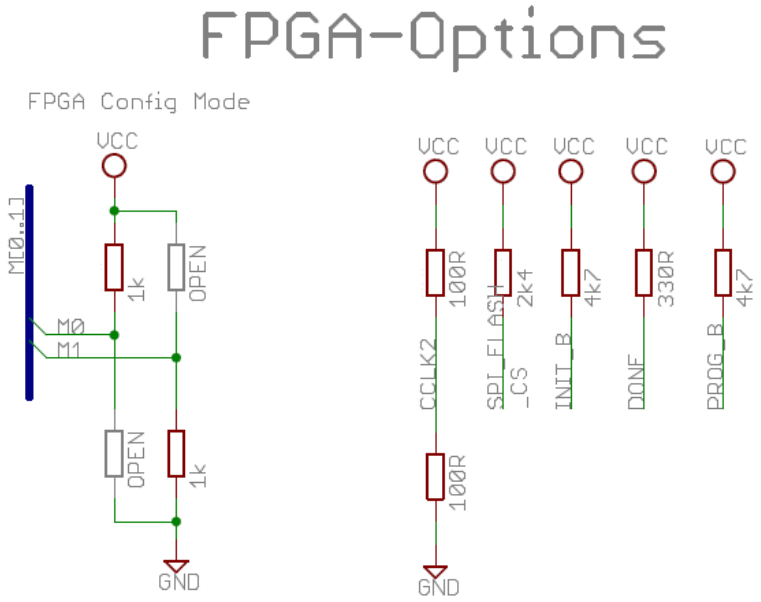
Layer		Material type	Description
	tStop	Dielectric	Solder mask top
1	**Top**	Conductive	Signal layer top
		Dielectric	Prepreg
2	**GND**	Conductive	Power plane GND
		Dielectric	Core
3	**Inner 3**	Conductive	Signal layer
		Dielectric	Prepreg
4	**Inner 4**	Conductive	Signal layer
		Dielectric	Core
5	**VCC**	Conductive	Power plane VCC
		Dielectric	Prepreg
6	**Bottom**	Conductive	Signal layer bottom
	bStop	Dielectric	Solder mask bottom

8 layer stackup

Layer		Material type	Description
	tStop	Dielectric	Solder mask top
1	**Top**	Conductive	Signal layer top
		Dielectric	Prepreg
2	**GND**	Conductive	Power plane GND
		Dielectric	Core
3	**Inner 3**	Conductive	Signal layer
		Dielectric	Prepreg
4	**VCC**	Conductive	Power plane VCC
		Dielectric	Core
5	**GND**	Conductive	Power plane GND
		Dielectric	Prepreg
6	**Inner 6**	Conductive	Signal layer
		Dielectric	Core
7	**VEE**	Conductive	Power plane VEE
		Dielectric	Prepreg
8	**Bottom**	Conductive	Signal layer bottom
	bStop	Dielectric	Solder mask bottom

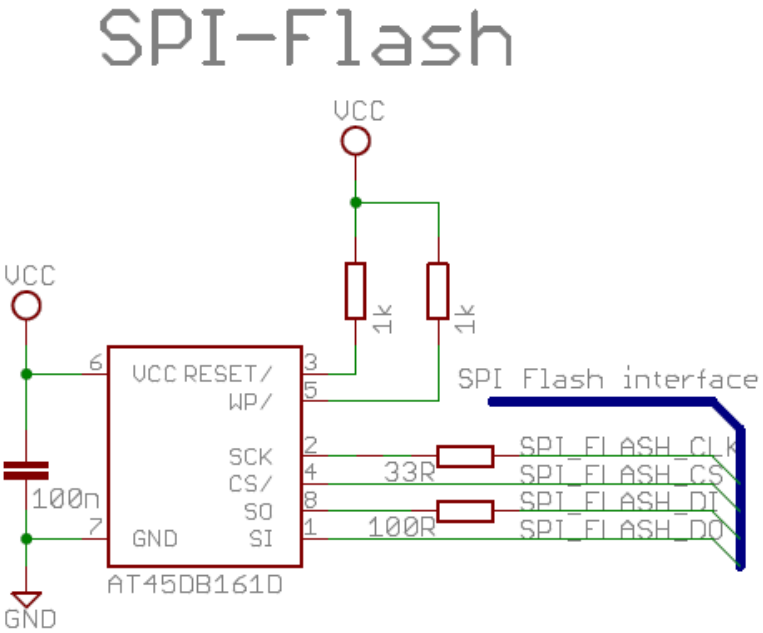
4.3.2 Configuration

The boot-up of the FPGA is configured via pull-up or pull-down resistors. The EasySlave reads the configuration from the serial flash device and starts direct the MicroBlaze application.



4.3.3 SPI-Flash (Config device)

For the EasySlave the AT45DB161(D) serial flash device from Atmel is recommended.



4.4 PHY selection [S2]

The operation of a sercos III network requires the observance of certain conditions with respect to the interaction of the used communication interface, including the sercos III Ethernet MAC and PHY components. These conditions are partly beyond the current standards, so that not every Ethernet PHY that is available in the market is suitable for use in a sercos III network.

FPGAs based on standard pin out (bitstream) supports only MII interfaces. IP core users are free to use also RMII interfaces. RMII is not recommended, because of a higher jitter and an increased delay on the device.

Some requirements should available without using the MII management interface. The features below have to be enabled after power on, e. g. by default or by strapping pins.

4.4.1 Basic features

- PHYs have to comply with IEEE 802.3 100BaseTx and/or 100BaseFX.
- PHYs have to provide an MII interface.
- PHYs have to use auto negotiation.
- PHYs have to support 100Mbit/s Full Duplex links.
- PHYs have to support MDI/MDI-X auto crossover.
- PHYs have to support the MII management interface.
- PHYs have to provide a signal for indicating a 100Mbit/s link.

The following characteristics can be found in the datasheet of the PHY component or be requested from the manufacturer. The candidate must support the following features:

- Transfer of 100 Mbps, full duplex
- Auto-negotiation
- Auto-MDIX (auto crossing)
- Automatic polarity detection and correction
- MDIO with MII Interface to the MAC, 3.3V LVTTL compatible
- Output of "False Carrier" signal on the MII interface
- Reference clock input 25 MHz (clock is supplied by MAC interface, e.g., FPGA)

A link output signal shall indicate the state of the links and responds quickly to the failure of the link.

For the EasySlave we recommend the PHY chip DP83848I from Texas Instruments (former National Semiconductor).

5 References

[S1] sercos Schematic for Xilinx Master/Slave Design_V1.3-0.8
https://wiki.sercos.org/rc-sys/wiki/images/rc-images/5/56/SCM_SERCON100_X_M_S_V1.3.0.8.pdf

[S2] sercos Phys Selection Guide
https://wiki.sercos.org/rc/Document/Phys

[X1] Spartan-6 FPGA Family Overview (ds160)
XILINX

[X2] Spartan-6 FPGA Datasheet – DC and Switching Characteristics (ds162)
XILINX

[X3] Spartan-6 FPGA – PCB Design and Pin Planning Guide (ug393)
XILINX

[T1] Datasheet – DP83848I
Texas Instruments